Jun 03, 1994 09:19 | GOPAL C. RAY | Chg_Scr

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```
=> s (interrupt request#) (p) idle
          48798 INTERRUPT
          28632 REQUEST#
           2611 INTERRUPT REQUEST#
                  (INTERRUPT(W)REQUEST#)
          32717 IDLE
L1           77 (INTERRUPT REQUEST#) (P) IDLE

=>
```

INPUT:

```
=> s interrupt# (p) state#
            59823 INTERRUPT#
           684425 STATE#
L7           9423 INTERRUPT# (P) STATE#

=> s interrupt# (p) idle
            59823 INTERRUPT#
            32717 IDLE
L8           1258 INTERRUPT# (P) IDLE

=> s l8/ab
             4009 INTERRUPT#/AB
             2654 IDLE/AB
L9             21 (INTERRUPT#/AB (P) IDLE/AB)

=>
```

INPUT:

```
=> s mask(p)(interrupt request#)
         55893 MASK
         48798 INTERRUPT
         28632 REQUEST#
          2611 INTERRUPT REQUEST#
                 (INTERRUPT(W)REQUEST#)
L1          289 MASK(P)(INTERRUPT REQUEST#)

=> s l1 (p) enable
        288494 ENABLE
L2          66 L1 (P) ENABLE

=>
```

INPUT:

```
=> s 4010448/pn or 4010448/uref or 5095526/pn
             1 4010448/PN
            11 4010448/UREF
             1 5095526/PN
L1           13 4010448/PN OR 4010448/UREF OR 5095526/PN

=> d 1-13
```

1. 5,095,526, Mar. 10, 1992, Microprocessor with improved interrupt response with interrupt data saving dependent upon processor status; Allen J. Baum, 395/725; 364/280.8; 395/775 [IMAGE AVAILABLE]

2. 4,777,591, Oct. 11, 1988, Microprocessor with integrated CPU, RAM, timer, and bus arbiter for data communications systems; Ki S. Chang, et al., 395/800; 364/DIG.1 [IMAGE AVAILABLE]

3. 4,635,188, Jan. 6, 1987, Means for fast instruction decoding for a computer; Donald A. Williamson, et al., 395/375; 364/231.9, 232.3, 243, 243.4, 244, 244.6, 244.9, 252.3, 252.6, 255, 255.1, 255.7, 259, 259.1, 259.9, 261.3, 262.4, 262.7, 262.8, 263, 265, 266.3, 271.6, DIG.1; 395/500 [IMAGE AVAILABLE]

4. 4,486,624, Dec. 4, 1984, Microprocessor controlled radiotelephone transceiver; Larry C. Puhl, et al., 370/24; 379/60; 455/77, 89 [IMAGE AVAILABLE]

5. 4,471,456, Sep. 11, 1984, Multifunction network; Michael H. Branigin, et al., 395/325; 364/232.8, 232.9, 238, 240, 240.1, 240.2, 240.5, 240.7, 241.9, 254, 254.3, 254.5, 255, 255.1, 259, 259.9, 265, 265.2, 266.3, 926.9, 927.8, 933, 933.2, 933.4, 935, 935.2, 935.4, 935.45, 935.46, 935.47, 939, 939.5, 943.9, 945.6, 947, 947.1, 948.1, 955, 955.3, 957, 957.6, 958.5, 959, 965, 965.9, 966, DIG.1, DIG.2 [IMAGE AVAILABLE]

6. 4,434,461, Feb. 28, 1984, Microprocessor with duplicate registers for processing interrupts; Larry C. Puhl, 395/725; 364/222.2, 222.3, 222.4, 231, 231.2, 231.3, 232.8, 234, 237.2, 237.4, 237.8, 241.2, 243, 243.7, 244, 244.6, 244.9, 247, 252, 259.9, 284, 284.2, DIG.1; 455/33.1, 73 [IMAGE AVAILABLE]

7. 4,425,616, Jan. 10, 1984, High-speed time share processor; Jack L. Woodell, 395/600; 364/222.2, 228.3, 228.4, 230, 230.3, 230.4, 231.4, 231.6, 231.7, 238.5, 240, 240.4, 243, 243.4, 243.41, 244, 244.6, 248.6, 258, 261.3, 261.4, 261.5, 265, 266.3, 268, 268.3, 268.8, 269.4, 270, 284, 284.1, 284.3, DIG.1; 395/375 [IMAGE AVAILABLE]

8. 4,398,265, Aug. 9, 1983, Keyboard and display interface adapter architecture; Larry C. Puhl, et al., 395/275; 364/919, 919.2, 919.4, 925.6, 926.1, 926.5, 927.2, 927.5, 927.8, 927.92, 927.98, 927.99, 928, 929, 931.3, 933, 933.2, 933.3, 935, 935.2, 935.3, 935.4, 935.6, 940, 940.1, 940.2, 942.7, 942.8, 946.2, 946.6, 947, 947.1, 948.1, 950, 950.3, 959.1, 964, 964.1, 965, 965.5, 965.8, DIG.2; 455/73 [IMAGE AVAILABLE]

9. 4,390,963, Jun. 28, 1983, Interface adapter architecture; Larry C. Puhl, et al., 395/325; 364/222.2, 222.3, 232.8, 234, 234.4, 237.2, 238.5, 240, 244, 244.5, 244.6, 254, 254.4, 919, 919.2, 919.4, 925.5, 925.6, 927.2, 927.5,

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INPUT:

US PAT NO: 5,282,272 [IMAGE AVAILABLE] L2: 2 of 46

BSUM(8)
originally sending the interrupt request at a high priority to ensure that it interrupts the processor it is directed to may not be the most efficient method.

US PAT NO: 5,249,284 [IMAGE AVAILABLE] L2: 3 of 46
US-CL-CURRENT: 395/425; 364/243, 243.41, 247, 265.3, 285, DIG.1

DETDESC:

DETD(14)

Referring to FIGS. 2A and 2B, REQ is active when the BUSB and MWRDY signals are an active "1" and at least TD0 or TD1 is a "1". The output of AND gate 50 is "1" and, in the idle condition, flip-flop 66 provides a Q/ output of "1". The output of AND gate 52 is "1", the Q/ output of flip-flop 58 goes to "0" to sample NOR gate 44 which is a "0", and the output of NOR gate 46 goes to a "1". This sets the Q/ output of flip-flop 62 to "0" which inverter 74 converts to a "1" (REQ). REQ is then transmitted to processor 12 as an interrupt request signal. Processor 12 acknowledges the request when it is ready to respond to an invalidation cycle by providing a high RESP signal. This drives the output of AND gate 48 high which sets the Q/ output of flip-flop 64 to a "0 " which is the output enable signal OEN/. Referring to FIG. 1A, OEN/ is received by address buffers 30 which place the address of the overwritten data block on the address line ABUSA of bus 14. Referring again to FIGS. 2A and 2B, the output of AND gate 56 is "1" which activates the address strobe signal AS/ so that the address on ABUSA is strobed into processor 12. The Q/ output of flip-flop 60 feedsback to AND gate 56 which resets the AS/ signal on the next CLK signal. The Q/ output of flip-flop 60 is also provided through inverter 72 to AND gate 54 and along with the Q output feedback from from flip-flop 64 resets flip-flop 64 and OEN/. The Q output of flip-flop 64 is also provided to the K input of flip-flop 62 to reset REQ at the same time AS/ is generated.

US PAT NO: 5,218,680 [IMAGE AVAILABLE] L2: 4 of 46
US-CL-CURRENT: 395/325; 364/231.8, 239.5, 241.9, 242.32, 260, 284.4, DIG.1; 370/53, 77, 85.1, 94.1; 395/200

DETDESC:

DETD(615)

RFM.sub.-- TS02 comprises a 16-bit field RFMFBC, indicating the number of bytes received by RFM relative to the respective channel during the current frame, and 16 reserved/unused bits. Upon detection of end of frame, idle or abort condition, RFM adjusts the value in RFMFBC (to ensure that CRC bytes are not included in the count), and the adjusted value together with the value of RFMIS in RFM.sub.-- TS01 are passed to (picked up by) INT during the latter's interrupt request handling process.

DETDESC:

DETD(730)

The R fields include four 1-bit "source" indications and six status indications; of the latter four are 1-bit parameters, one is a 4-bit parameter, and the remaining one is a 16-bit term. The source indications

INPUT: